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METHODS AND COMPONENTS FOR OPTICAL CONTENTION RESOLUTION IN HIGH SPEED NETWORKS

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CONSORTIUM EXECUTIVE SUMMARY

During the second quarter of this project the consortium members focused their activities on continuation of experimental design, implementation of results obtained so far in system analysis effort, and integration of the CRO (Contention Resolution Optics) module. Still much time was spent on component selection and ordering and reconciling differing vendor supplied performance specifications. A detailed evaluation of performance and functionality required was used to fine tune the design of logic operations and the optical modules. Some modifications are needed in light of experimental characterization work with more experiments and measurements in progress.

Work at GTE Laboratories focused on developing and building the CRO module. The sub-modules in progress are the header detector, polarization monitor, optical amplifiers and optical digital switches. To be functional in this application these parts must have low loss and low back reflection characteristics. This requires special packaging practices to be used in optical interfaces and splicing procedure was developed to reduce back reflections to below 50 dB. High speed header detector sub-module has been developed and is right now in a characterization stage. Completed is also design and part fabrication for enhanced thermal stability semiconductor optical amplifier. Because of its suitability for multifiber coupling, this approach will also be used in packaging of optical switches.

At Stanford University work in design and development of the CORD project prototype and sub-systems was continued. In particular, assembled and evaluated in performance were the data and header transmitters and receivers. Work also continued in the data traffic generation and recovery logic sub-systems, design and simulation of the circuitry required for header channel clock recovery. In addition, extensive theoretical analysis and computer simulation were performed in the optical and microwave signaling portions of the prototype.

Experimental time domain eye diagrams and frequency spectra of the header and data channels have been obtained and match well with simulation results. Crosstalk between the data and header channels has been alleviated by the use of data prefiltering. The microwave system of the optical transceiver for 2.488 Gbps data channel and 80 Mbps header channel has been built and tested. The system is using subcarrier multiplexing and frequency shift key (SCM-FSK) for the header channel. The stability of the voltage controlled oscillator (VCO), used for the SCM-FSK, was measured and its influence on the channels' bit error rate (BER) was evaluated.

A 80 Mbps prototype header generation logic board was built and used to evaluate the SCM-FSK transmitters. The header synchronization method, using multi-tap delay-lines and programmable logic devices (PLDs), has been designed, simulated, and is currently being assembled with on a wire-wrap board. The circuitry required for the inter-node slot synchronization has been designed and the necessary components ordered. A new chip-set, used to convert the 2.488 Gbps serial data traffic to parallel format, has been selected for the data transmitter and receiver portions of the prototype. Initial circuits are being built to verify the performance of the chip-set. The high level design of the traffic generator/detector and performance monitor logic has been completed and a PLD family with sufficient performance selected.

In the area of theoretical analysis, the power margin of the system including contention resolution optics (CRO) has been calculated and the optimal power ratio between data,

header, and clock pilot tone has also been determined. Computer simulations were used to assist in these calculations as well as in the selection and design of the filters required in both the transmitter and receiver portions of the prototype.

UMass activity during the second quarterly period of the project has provided new and original results concerning CORD operation, and prepared the basis for the development of a tool simulator. This tool will be the basis for validating current and future CORD network architectures and protocols, and will be used for a comprehensive comparison of alternative optical solutions. Following are the tasks completed within this time frame: A no-cost extension of improved Quadro-CORD contention resolution subsystem. Analytical models of the ring topology, required for independent validation of the generalized simulator. Evaluation of alternative simulation tools supporting the decision to develop of a customized tool for configuring optical network simulation models, designing access protocols and obtaining network performance results.

A large number of recent works, including this proposal, deal with the combined use of fiber delay lines and optical 2x2 switches to achieve a purely optical data transit solution based on time/space packet switching. In this approach the optical path length for packets passing the switch can be adjusted dynamically, by using a different number of delay lines as temporary optical storage. This makes it possible to resolve output link contentions arising among packets arriving at the switch from different input links or different wavelength channels. While the quality of performance in this solution is an increasing function of the optical storage capacity of the switch, its cost is linearly proportional to the number of optical 2x2 switches required by the switch design.

During the preceding quarter we investigated an extension of the proposed time/space switch architectures derived from the Quadro switch, which carries the potential of improving the contention resolution capacity of CORD without increasing its cost. We have shown that this effect is possible by increasing the optical storage capacity of the delay lines in the switch without increasing the number of optical switches. It has been shown that the proposed approach leads to a significantly better performance with no increase in cost.

Two network topologies are being considered in the framework of the CORD prototyping, a star and a ring. The star topology approach was the originally proposed network where contention resolution is achieved by means of Quadro, and has been already extensively studied in the past by the UMass research group. Several star network scenarios were studied and modeled with validated, approximate, Markov Chain based analyses. The ring topology was, on the other hand, proposed and fully developed only in the context of the current proposal, as the growing success enjoyed by optical amplifiers made compensation for insertion losses encountered at intermediate nodes possible in principle. To better understand the behavior of the control strategies and of the entire ring system we recently proposed several original analytical models, one for each control strategy. These models analyze capacity, throughput and end-to-end packet delay for the ring network equipped with Quadro user network interfaces. These Quadro interfaces allow packet contention resolution to be optically realized at both source and destination nodes. One analytical model for each control strategy was worked out, depending also on the location at which contentions are resolved, i.e., at the receiver node,or the transmitter node. All approximate analytical models were validated through comparison with simulation, showing a practically valid match with the simulation of the actual system behavior. These models will be usable for a quick analysis of alternatives during the design phase of alternative ring systems in this proposal, and as validation tools for the customized simulator.

To simulate the proposed (multi-wavelength) ring and (multi-wavelength) star networks we have considered a number of leading commercially available simulators. The related options were either the direct use of one of these tools, or the design of a new simulator based on an

existing commercial tool. The major commercially available packages considered in this phase were OPNET by MIL 3 Inc. and Bones by COMDISCO Systems, Inc. Both packages provide sophisticated tools for network performance evaluation; however, their main strength is on mobile and radio networks, ATM, Ethernet, and FDDI. The components that are being used currently in all-optical networks have been developed only very recently. As a result, there are not yet integrated in commercially available simulators. Consequently, the use of a commercial simulator does not offer any significant advantages over any other existing simulation package. To simulate multi-ring/multi-star architecture as well as the different networks selected for comparison we have therefore decided to use the already existing software tool ETS (Estelle translator-simulator) designed earlier at the University of Massachusetts. This tool was originally designed on the basis of a generally available CONSIP-II simulation tool, and it has the advantages of accepting a formal specification language for the description of protocols, as well as being open and therefore easy to be adapted for extensive use in all-optical network design and evaluation.

The UMass team is currently working on achieving new results for the improved design and implementation of Quadro performance in ring topologies. The study of multi-receiver user-network interface architecture combined with newly proposed control strategies to maximize throughput of packets successfully received by a multi-receiver user is currently undergoing. Further, the adaptation of multi-packet length delay lines proposed for Quadro in the two stage CORD prototype to improve its probability of contention resolution and packet loss performance is being investigated. The following list provides a partial description of the main efforts for the next quarter at the UMass networking laboratory:

Definition of distributed strategies for the ring topology and their evaluation.

Adaptation of the multi-packet length DLs approach for CORD prototyping.

Definition of strategies for multi-receiver Quadro in stations requiring large amount of data exchange, which exceeds the single channel data rate.

Study of the physical layer software module, suitable for optical and all-optical networks description and simulation. Definition of the software interface with the already existing simulator tools developed at UMass, i.e., CONSIP and ETS.

The section below contains the technical report of GTE Laboratories only. Stanford University and University of Massachusetts will submit their reports separately.

1. TECHNICAL SUMMARY

1.1 INTRODUCTION

The effort in construction of the CRO module included this month work in further development of the particular submodules, their characterization and fine tuning of design parameters. Moreover, design of the complete physical box with its inputs, controls and thermal considerations has been in progress. The optical amplifiers' cooling and the mechanical stability of the various parts were taken into account. Detailed measurements of the back reflections were performed and improvements in assembly or integration techniques derived. We keep in mind that the CRO box will be transported to Stanford and must be built not as a laboratory demo, but rather as a transportable item. This requires securing components and fibers, and affects the overall design of the box.

1.2 PREPROTOTYPE INTEGRATION

Emphasis in the assembly effort is on compatibility of the completed device with system performance requirements. This includes minimization of losses and reduction of back reflections. In the single polarization preprototype this also includes methods to minimize polarization cross-talk. Back reflections at optical interfaces were measured using HP reflectometer (model # 8504) which provides information on the level of back reflected power and the location of the reflecting surface. The header detector optical chip is shown below followed by the HP instrument trace.

HEADER DETECTOR

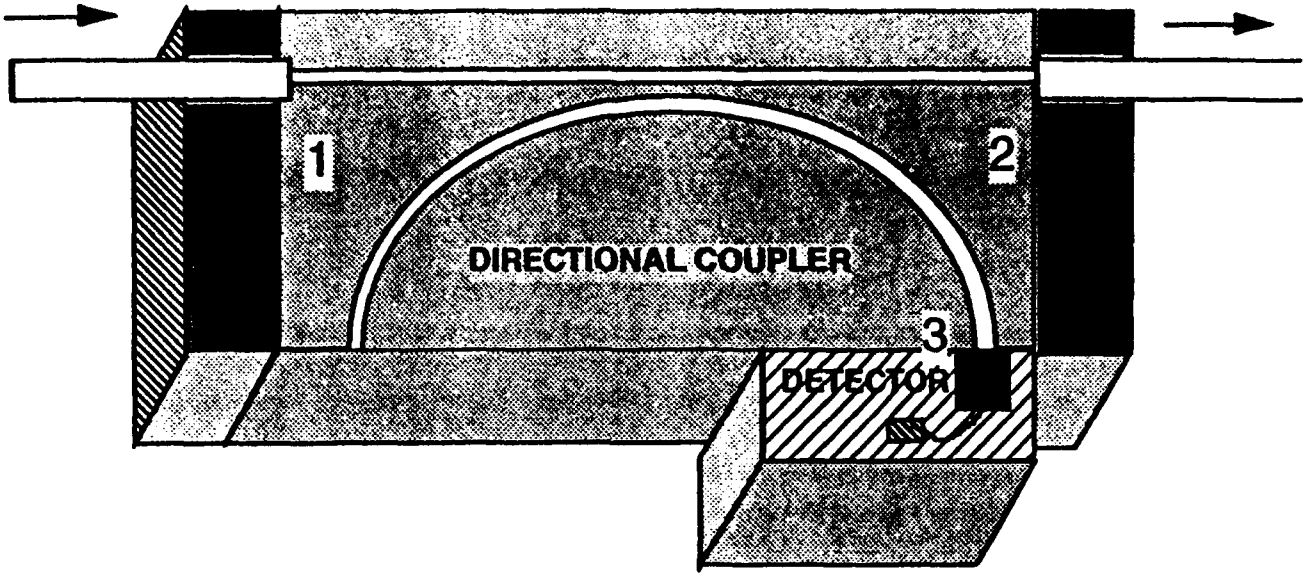
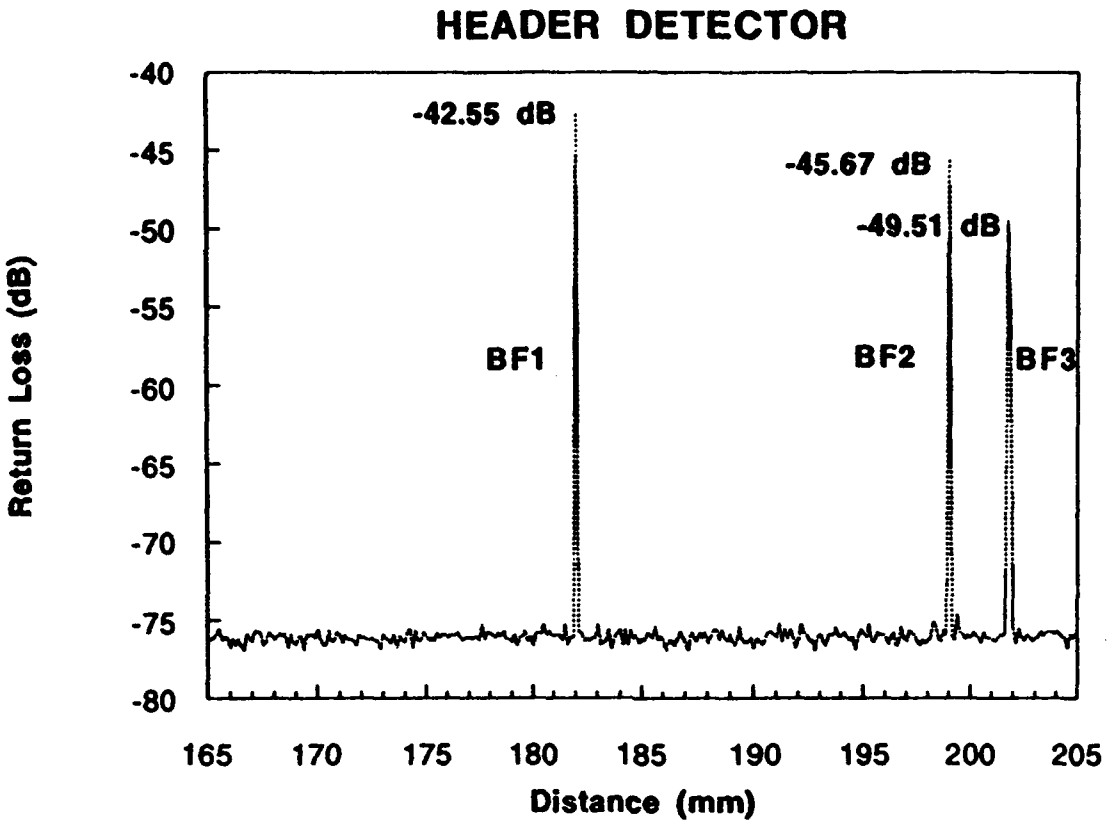
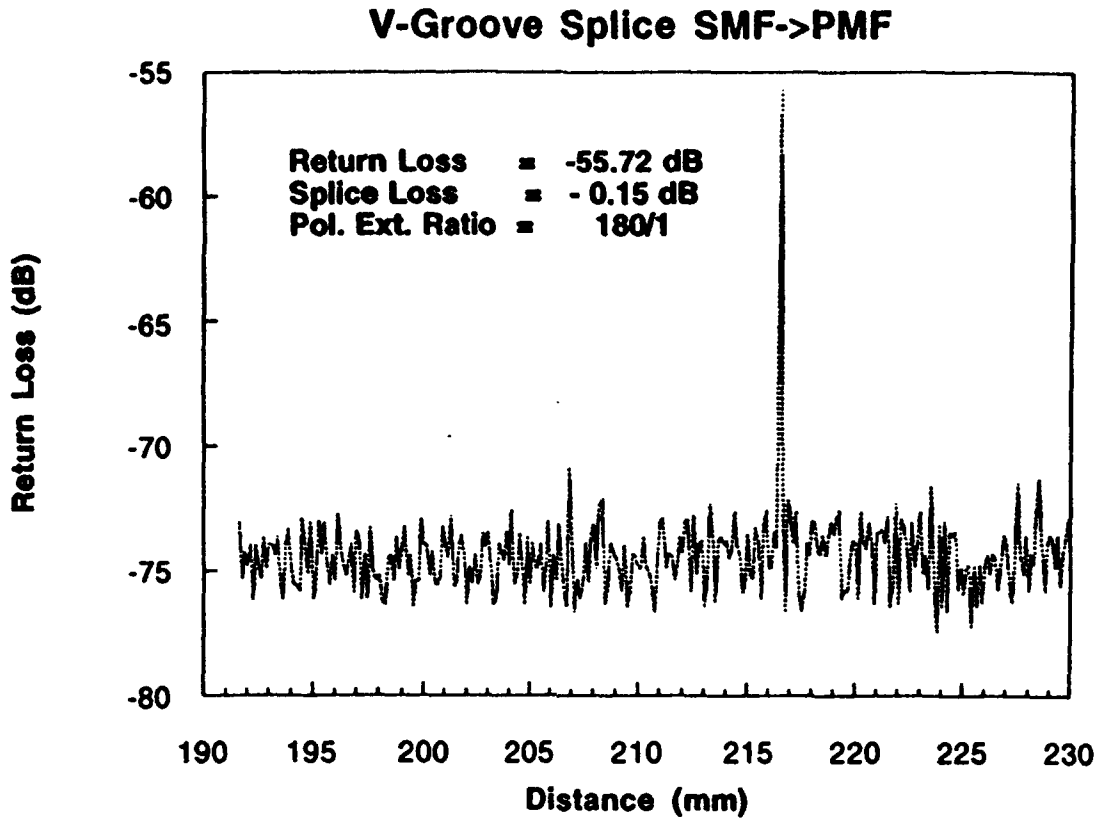


Figure 1. Header detector assembly. Fibers are secured in silicon v-grooves and are attached to a directional coupler chip. The high speed detector is surface mounted on the silicon, overlaying another v-groove which terminates underneath the active area of the detector with a reflecting angled surface.

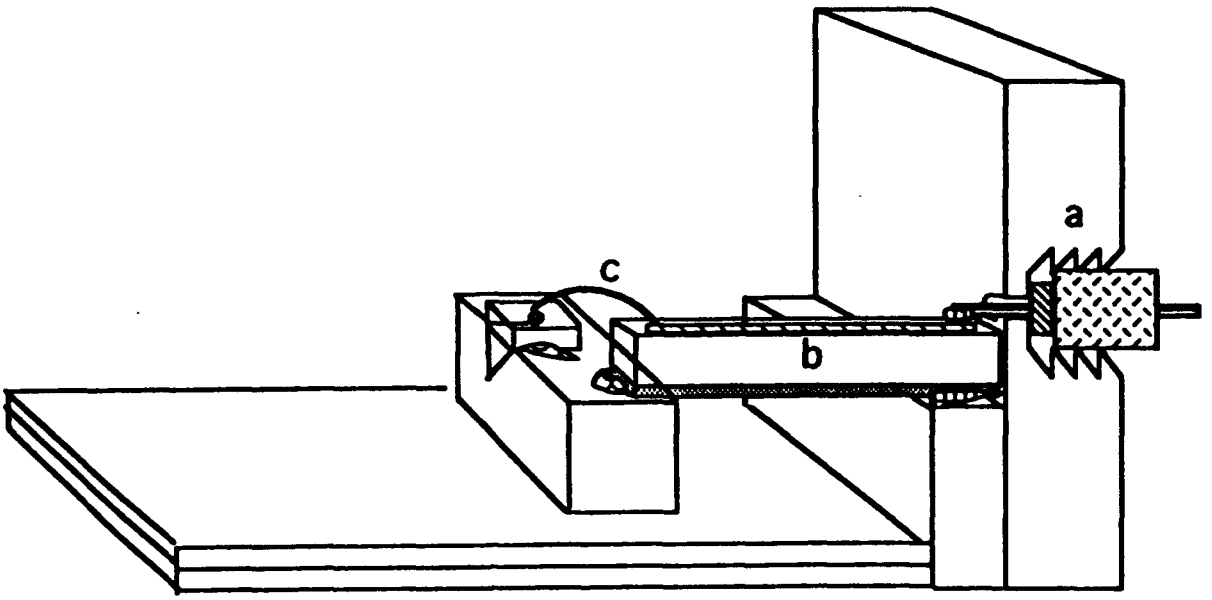


The CRO preprototype includes two types of fiber, single mode and polarization maintaining. Splicing of fibers inside the CRO enclosure required to develop techniques that produce low loss, low back reflections and low polarization cross-talk. The method used to perform this task was using silicon v-grooves which allow axial orientation to be made during the splicing operation. A trace of a splice backreflected level is shown
below.



A high speed header detector test package is shown below. The detector has been wirebonded to a microstrip and an SMA connector to provide detector output. Testing of this unit is in progress.

High Speed Detector Test Package



a. High speed electrical interface

b. Micro-strip conductor connecting package to detector

c. Critical wirebond to detector surface

1.3 DIGITAL OPTICAL SWITCH

The first step towards the development of the semiconductor digital optical switch was to fabricate and test 1X2 test structures. This was successfully completed with an extinction ratio of >20 dB between the output switching arms by the beginning of this ARPA project. The next step, fabrication and testing of 2X2 test structures, began in August of '93 with the design of the mask set. The completed mask set was received in October '93 from the mask vendor. A few initial fabrication runs were made with this new mask set on VPE-grown material. Primary goal was to determine the appropriate active layer and cladding layer thicknesses to assure single mode operation of the switch. In November '93, two MOCVD-grown wafers were ordered from EPI in England having the proper layer thicknesses as determined in the previous month.

The material structure has 0.32 μm thick active InGaAsP layer and 0.33 μm thick InP cladding layer. These layers are significantly thinner than the previous wafers and showed

superior single mode characteristics. Tests to determine the switching behavior of these devices are underway.

A new mask set for optical switches having curved waveguides to achieve a separation of 150 μm between the waveguide arm ends has been partially completed. This will permit packaging of the switch with two input and two output fibers. The fibers will have to approach at an angle of about 21 degrees from the facet normal due to the bending of light, whereas the waveguides will terminate at an angle of 7 degrees. The purpose of the 7 degree angle is minimization of internal reflections, a critical requirement for broadband optical components.

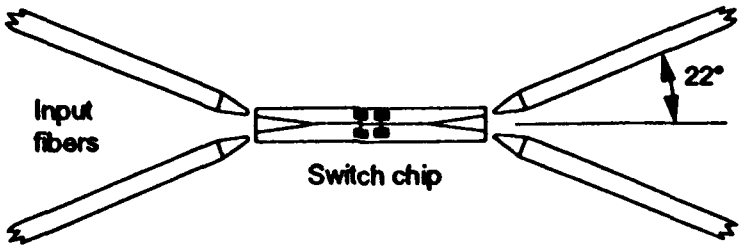


Figure 1. The 2x2 optical switch has on-chip input and output waveguides angled at 7° to the facet to minimize reflections. Refraction produces entrance and exit angles of about 22°.

1.4 AMPLIFIER PACKAGING

Both the semiconductor optical amplifier and the 2x2 switch will require multiple fiber alignments during packaging. Early optical amplifier packages, which used solder to fix fibers in place after alignment, have exhibited alignment-drift with time, and are not stable enough for long-term operation outside the laboratory environment. Maintaining alignment of two or more fixed fibers within fractions of a micron during package assembly, and over the device lifetime has proven difficult.

Therefore, a new approach is being developed which will allow fiber alignment to be finely adjusted after the fiber is fixed in approximately the correct position. This fine alignment can also be used to correct for drift which may occur with time. This packaging concept will result in a somewhat larger housing than would a non-adjustable approach. However, it is intended as a means to supply advanced components for subsystem and test bed development in a timely and cost-effective manner. Fabrication of prototype fiber alignment mechanisms incorporating this fine-adjustment approach is currently under way.

2 FUTURE PLANS

Activities in the next quarter will focus on finalizing fabrication of a number of components including the header detector, polarization monitors, packaging of optical amplifiers and operation of the digital optical switch. Moreover considerable effort will be devoted to assembly of all the parts comprising the CRO module. This effort will include fine tuning of assembly techniques, characterization of the assembled submodules, provision of electrical outputs and controls and assuring low loss operation. In addition, heat removal from the amplifiers will be incorporated into the module physical design. Securing the stability of components for transportation to Stanford will be an important consideration in the final design.

3. MILESTONES

No milestones were scheduled for the first quarter of this project for GTE Laboratories.